1. Device Overview

Die

Module

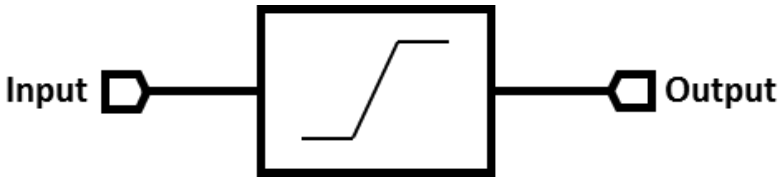
1.1 General Description

The HLM-40 is a high-power GaAs Schottky diode signal limiter featuring high IP3 and high power handling. It offers low insertion loss and low return loss from DC through Ka band and has a typical 1dB compression point of 15dBm. Its high power handling makes it ideal for protecting sensitive components and for applications requiring high linearity. It is available as a wire bondable die and as a connectorized module.

1.2 Features

- DC to 40 GHz limiter
- 20W Peak Power (pulsed), 4W CW
- 18dBm Flat Leakage @ 1W CW
- Typical P1dB of 15dBm
- Small signal S2P data: HLM-40U.zip, HLM-40CH.zip

1.3 Functional Block Diagram



1.4 Part Ordering Options[1]

Part Number	Description	Package	Green Status	Product Lifecycle	Export Classification
HLM-40CH	Wire bondable die	CH	**RoHS**	Active	EAR99
HLM-40U	Connectorized module	U		Active	EAR99

[1] Refer to our website for a list of definitions for terminology presented in this table.

Table of Contents

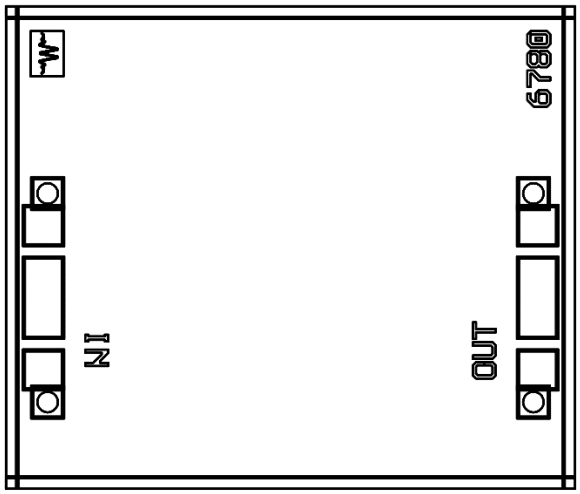
Revision History

Revision Code	Revision Date	Comment
-	September 2019	Initial Release
A	October 2019	Corrected References
B	December 2019	Updated sect. 3.4 Graphs

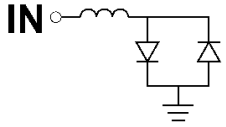
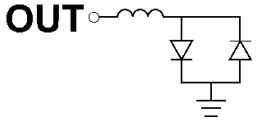
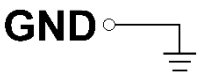
2. Port Configurations and Functions

2.1 Port Diagram

A top-down view of the HLM-40's CH package outline drawing is shown below. The HLM-40 has the input and output ports given in Port Functions.



2.2 Port Functions

Port	Function	Description	Equivalent Circuit for Package
IN	Input	The input port is diode connected for the CH and U package.	
OUT	Output	The output port is diode connected for the CH and U package.	
GND	Ground	CH package ground path is provided through the substrate and ground bond pads. U package ground provided through metal housing and outer coax conductor.	

3. Specifications

3.1 Absolute Maximum Ratings

The Absolute Maximum Ratings indicate limits beyond which damage may occur to the device. If these limits are exceeded, the device may be inoperable or have a reduced lifetime.

Parameter	Maximum Rating	Units
Average Power Handling at input port[2,3]	4	W
Peak Power Handling at input port[3]	20	W
Operating Temperature	-55 to +100	°C
Storage Temperature	-65 to +125	°C

3.2 Package Information

Parameter	Details	Rating
ESD	Human Body Model (HBM), per MIL-STD-750, Method 1020	1A
Weight	U Package	10 g

3.3 Linear Regime Electrical Specifications

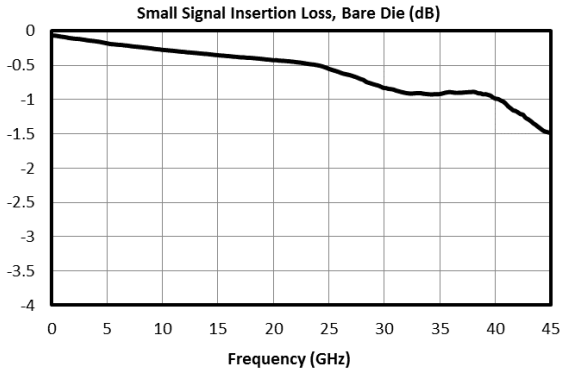
The electrical specifications apply at T_A=+25°C in a 50Ω system. Typical data shown is for the connectorized U-package limiter unless otherwise specified. Linear Specifications valid for input power up to the 0.1dB compression point. See page 5 for P0.1dB graph.

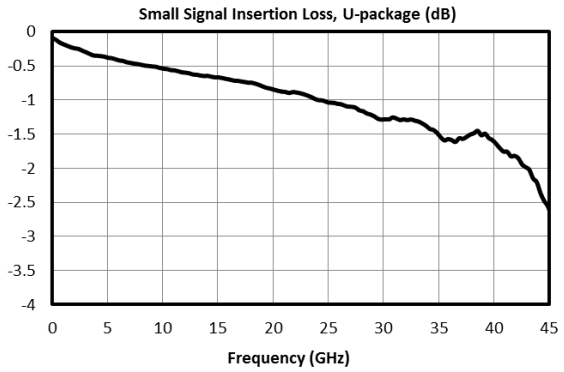
Min and Max limits are guaranteed at T_A=+25°C.

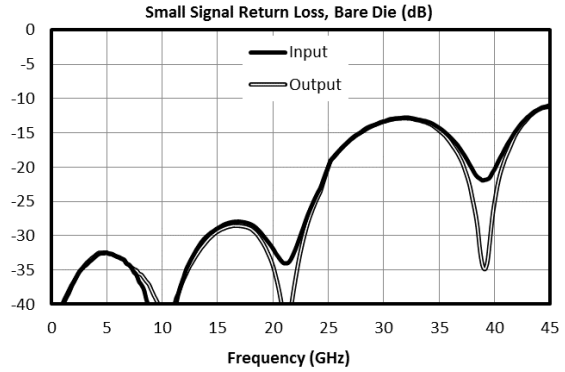
Parameter	Test Conditions	Min	Typical	Max	Units
Insertion Loss, bare die	DC – 40GHz		0.5	1.5	dB
Insertion Loss, U package			1	3	
Return Loss, bare die			26		dB
Return Loss, U package			14		
Flat Leakage at 1W			18		dBm
Input IP3 (IIP3)			See graph		dBm
Input 1dB Gain Compression Point (P1dB)			15		dBm
Recovery Time[4]			10		ps

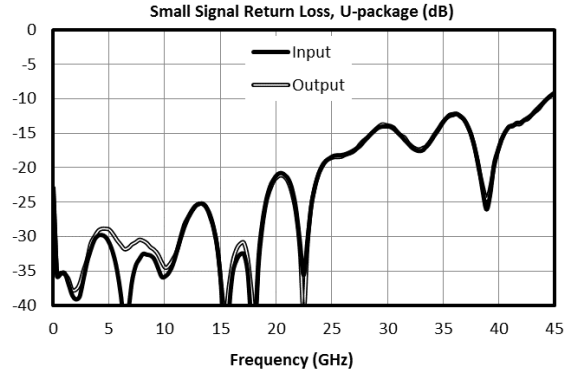
[2] Average power handling derated linearly to +35dBm at 85°C. Power handling spec based on observed power handling at 800MHz. Actual power handling is frequency specific.
[3] See section 3.5 for basis of power handling specs.
[4] Calculated based on equivalent capacitance and resistance.

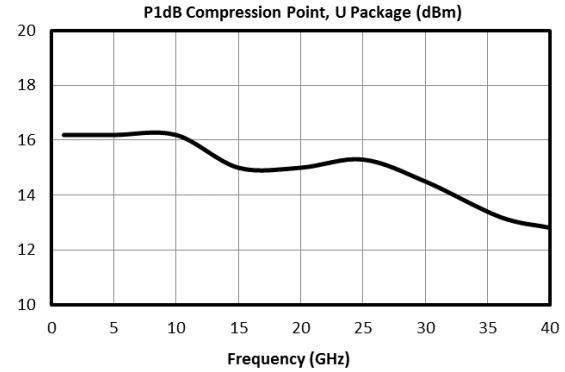
3.4 Typical Performance Plots

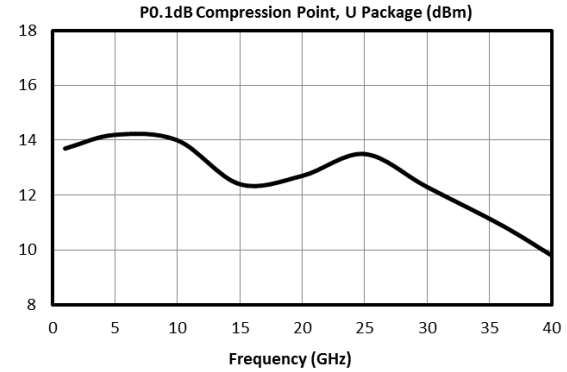


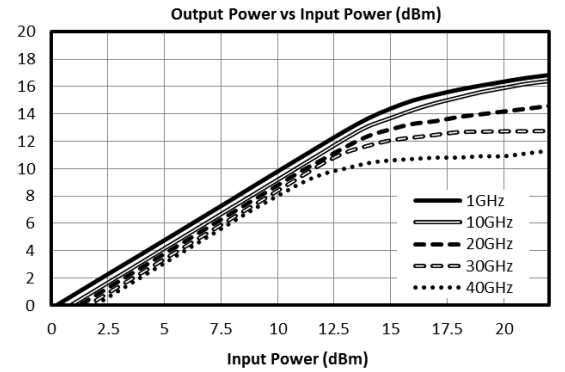


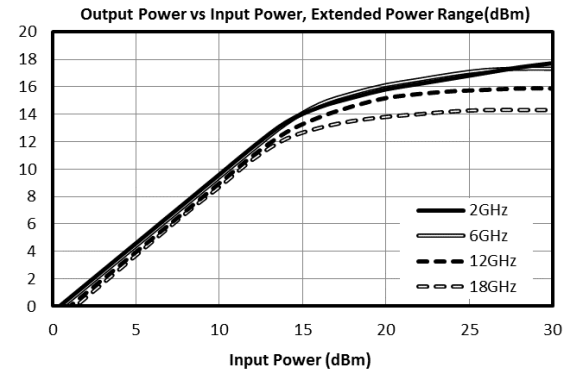


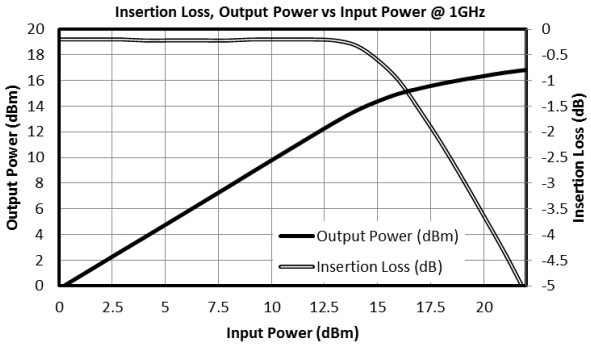


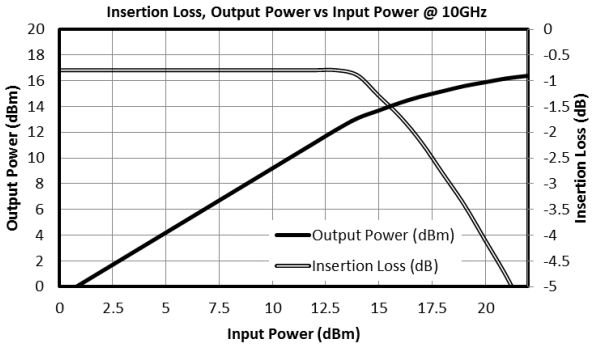


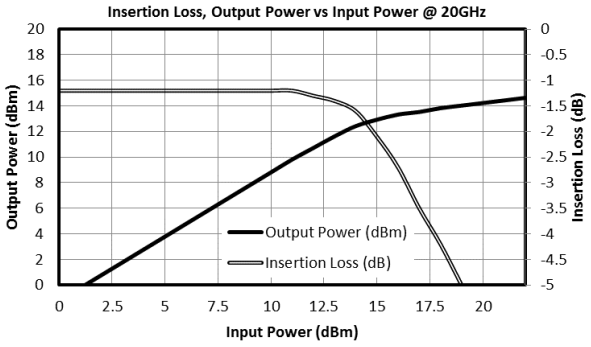


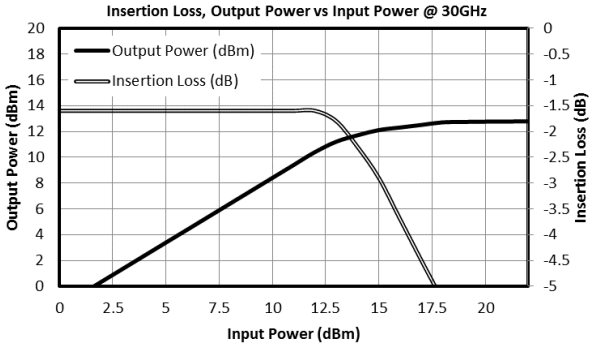


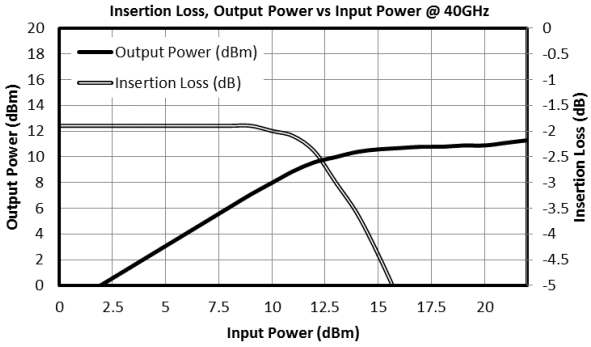


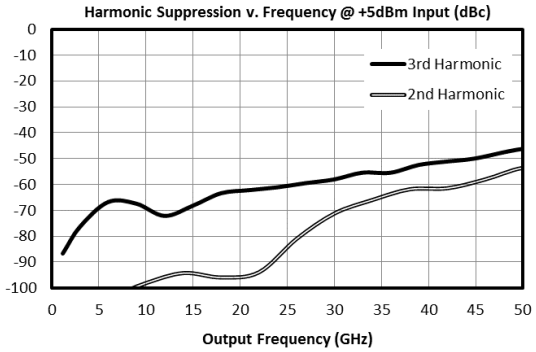


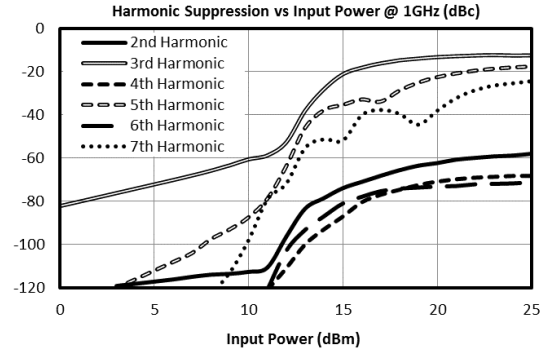


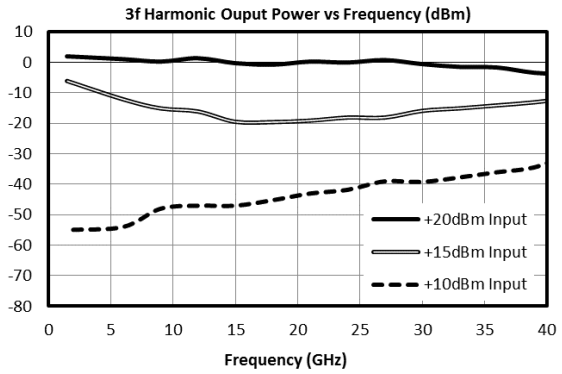


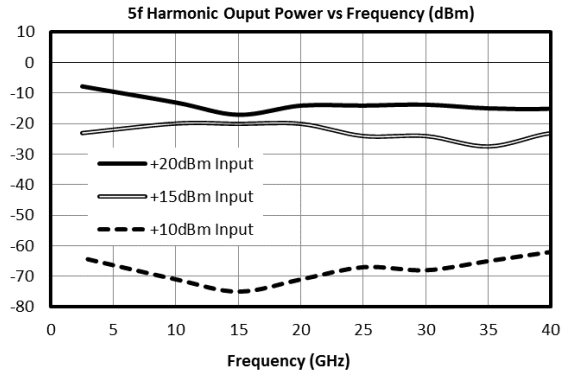


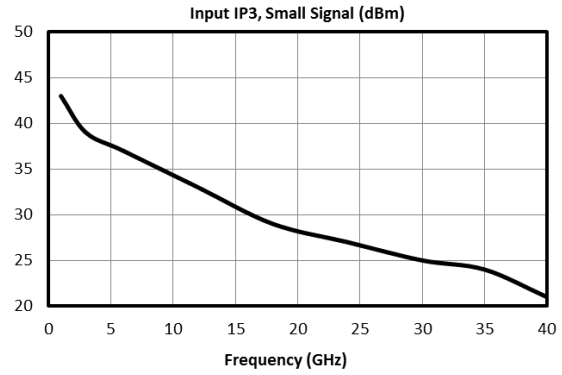


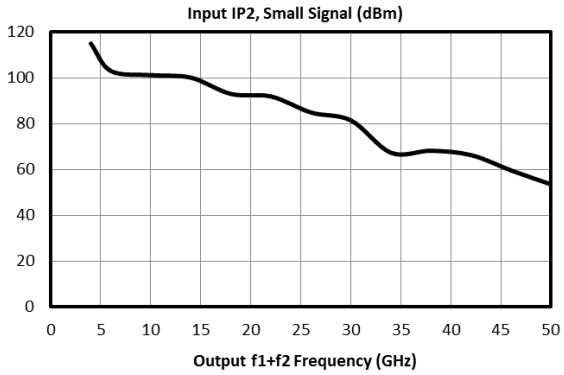












3.5 Input Power at Observed Failure

Power handling specification is based on tests performed at different combinations of temperature and frequency. Input power was increased until catastrophic failure was observed. Results are shown in the following table. The power handling specification listed in section 3.1 is based on the worst observed power handling derated by 3dB.

Frequency	Maximum Average Power Handling		Unit
	at 25°C	at 85°C	
0.8 GHz	39	38	dBm
2.5 GHz	42	41	
6 GHz	40	39	

Frequency	Maximum Peak Power Handling[5]	Unit
2 GHz	35	W

[5] Tested using a 1µs pulse, 1% duty cycle at 25°C

4. Die Mounting Recommendations

4.1 Mounting and Bonding Recommendations

Marki MMICs should be attached directly to a ground plane with conductive epoxy. The ground plane electrical impedance should be as low as practically possible. This will prevent resonances and permit the best possible electrical performance. Datasheet performance is only guaranteed in an environment with a low electrical impedance ground.

Mounting - To epoxy the chip, apply a minimum amount of conductive epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip. Cure epoxy according to manufacturer instructions.

Wire Bonding - Ball or wedge bond with 0.025 mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31 mm (12 mils).

Circuit Considerations – 50 Ω transmission lines should be used for all high frequency connections in and out of the chip. Wirebonds should be kept as short as possible, with multiple wirebonds recommended for higher frequency connections to reduce parasitic inductance. In circumstances where the chip more than .001" thinner than the substrate, a heat spreading spacer tab is optional to further reduce bondwire length and parasitic inductance.

4.2 Handling Precautions

General Handling

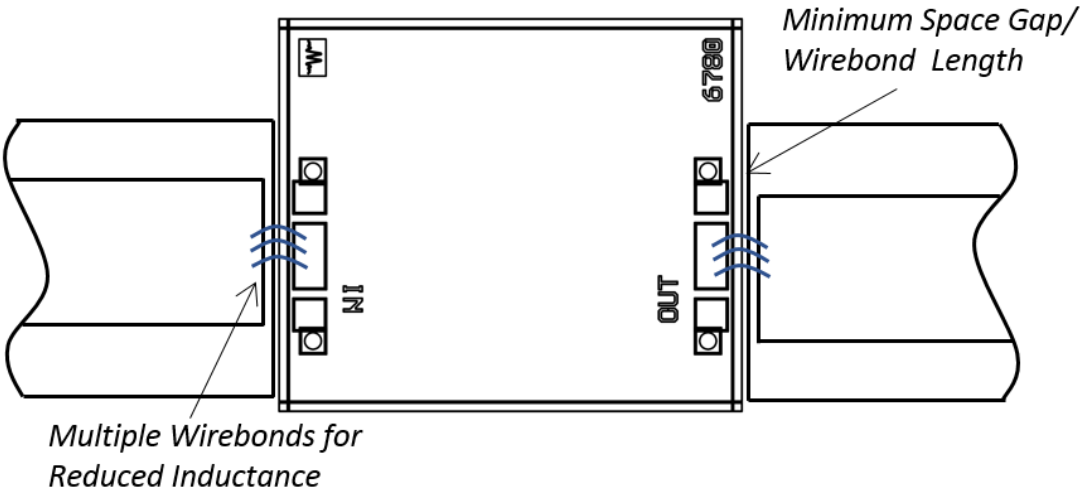
Chips should be handled with care using tweezers or a vacuum collet. Users should take precautions to protect chips from direct human contact that can deposit contaminants, like perspiration and skin oils on any of the chip's surfaces.

Static Sensitivity

GaAs MMIC devices are sensitive to ESD and should be handled, assembled, tested, and transported only in static protected environments.

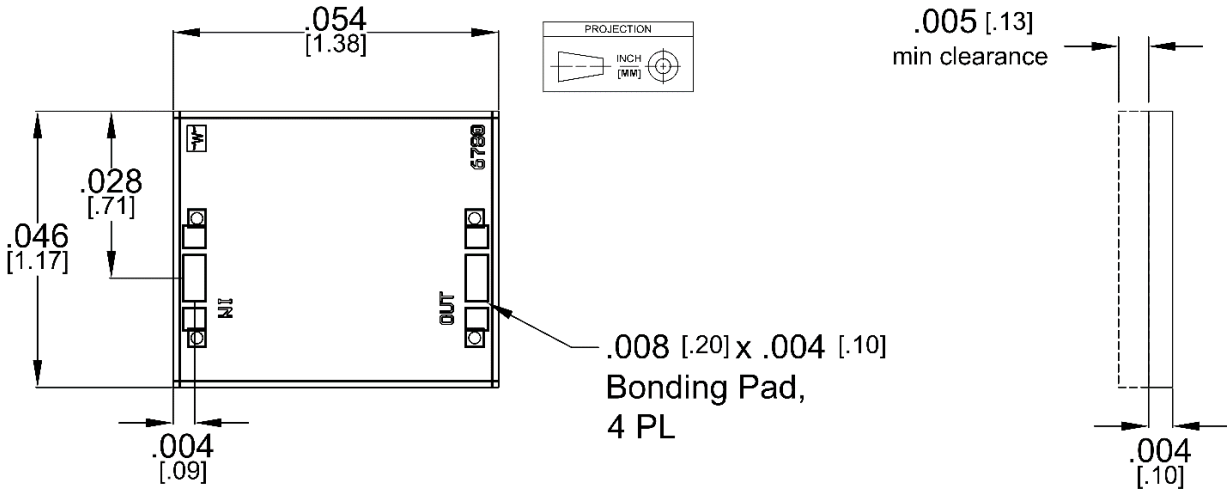
Cleaning and Storage: Do not attempt to clean the chip with a liquid cleaning system or expose the bare chips to liquid. Once the ESD sensitive bags the chips are stored in are opened, chips should be stored in a dry nitrogen atmosphere.

4.3 Bonding Diagram



5. Mechanical Data

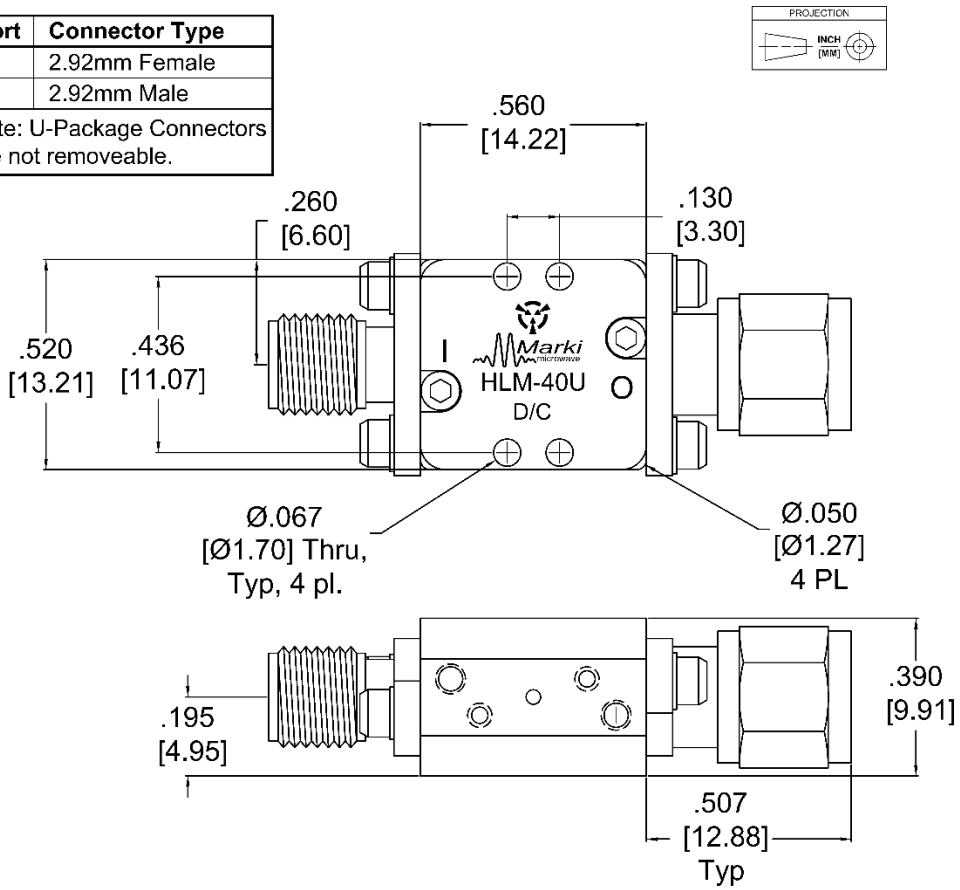
5.1 CH Package Outline Drawing



1. CH Substrate material is 0.004 in thick GaAs.
2. I/O trace finish is 4.2 microns Au. Ground plane finish is 5 microns Au.
3. Tolerance for X, Y dimensions is ±0.002 in. Tolerance of metallization is ±0.0001 in.

5.2 U Package Outline Drawing

Port	Connector Type
I	2.92mm Female
O	2.92mm Male
Note: U-Package Connectors are not removeable.	



Unless otherwise specified, dimensions are in inches. Tolerances are:

.XX ± .02
.XXX ±.005